

Electron-beam SAFIER™ process and its application for magnetic thin-film heads

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(Received 2 June 2004; accepted 21 September 2004; published 13 December 2004)

We have coupled the SAFIER™ (shrink assist film for enhanced resolution) process with electron-beam lithography for the fabrication of the write top pole structures for thin-film heads. The SAFIER™ process is designed to physically shrink trench patterns and contact holes with very little deterioration of the resist profile. In this article, we will present the experimental results of the SAFIER™ process for the fabrication of the write top pole. We investigate the SAFIER™ process concerning several key processing issues, including shrink resolution capability, repetition of the SAFIER™ process, shrink-sensitive baking conditions, resist sidewall profile, and line edge roughness (LER) after shrinking of the trench. The experimental results show that this process not only shrinks the size of resist trenches and contact holes, but also improves LER and critical dimension variation. We demonstrate the capability of printing top pole structures with pole widths of sub-20 nm in a 0.30- μm -thick resist (aspect ratio > 15:1), and electroplated top pole structures of 50 nm in a 0.50- μm -thick resist (aspect ratio = 10:1). © 2004 American Vacuum Society.
[DOI: 10.1116/1.1815309]

I. INTRODUCTION

The areal density in the data storage industry has sustained annual increases as high as 100% over the last five years.^{1,2} To elevate areal density to 1 Terabit/in.² and beyond we need to shrink the critical features of recording devices, e.g., writer top poles and read sensors, down to the 30 nm regime. One of the processing challenges is to fabricate these 30 nm features with high aspect ratio (AR). To achieve this we previously developed various high-AR narrow trench processes using electron-beam lithography.^{3,4} In this article, we report an approach using a size shrinkage method to reduce the trench critical dimension (CD) with a high AR.

Size shrinkage technologies have recently attracted much attention due to the difficulty in pushing small CDs and the extremely high cost of tools. Size shrinkage technologies achieve next-generation level pattern sizes by combining various additional processes with conventional lithography. There are typically two main shrinkage techniques that people currently use in lithography. One is the resist thermal flow process, which is performed by high-temperature heat treatments,⁵ and the other is the chemical shrink process in which a mixing layer is formed by utilizing the crosslinking reaction catalyzed by the acid component existing in a pre-defined resist pattern.⁶ Very recently, Tokyo Ohka Kogyo (TOK) Co., Ltd. introduced a size shrinkage process called SAFIER™ (shrink assist film for enhanced resolution).⁷ SAFIER™ is an extraordinary process that enables aggressive CD targets for KrF, ArF, electron-beam contact holes, and trench features. In this article, we present the experimental results of the electron-beam SAFIER™ process for write top pole structures. We investigate the SAFIER™ process

concerning several key processing issues, including shrink resolution capability, repetition of the SAFIER™ process, shrink-sensitive baking conditions, resist sidewall profile, and line edge roughness (LER) of the trench after shrink. The experimental results show that this process not only shrinks the size of resist trenches and contact holes, but also improves LER and CD variation. We demonstrate the capability of printing top pole structures with pole widths of sub-20 nm in a 0.30- μm -thick resist (AR > 15:1), and electroplated top pole structures of 50 nm in a 0.50- μm -thick resist (AR = 10:1).

II. EXPERIMENTAL PROCEDURE

UV113, a chemically amplified resist from Shipley Corporation, was used with 6 in. round silicon wafers for the evaluation of the SAFIER™ process. Exposure was performed using a Leica VB6 direct write vector beam lithography system operating at 50 keV with an 800 μm field and 12.5 nm grid size. The exposed wafer was post-exposure baked at 130 °C for 60 s, and developed using standard 0.263 N tetra methyl ammonium hydroxide developer (Shipley LDD-26W) in a single puddle process on an FSI 2000 cluster tool. Top-coating material FSC-8000GM (200–300 nm thick) was purchased from TOK for the SAFIER™ process. Electrodeposition was implemented using a standard Permalloy™ plating bath with a pulse plating process. Atomic force microscopy (AFM) measurements were performed in tapping mode with a Dimension 2500 system (Veeco Digital Instruments). Scanning electron microscopy (SEM) characterization was conducted using a dual-beam focused ion beam (FIB)/SEM from FEI Corporation. Automatic top-down CD measurements were taken with the VeraSEM three-dimensional (3D) system (Applied Materials, Inc).

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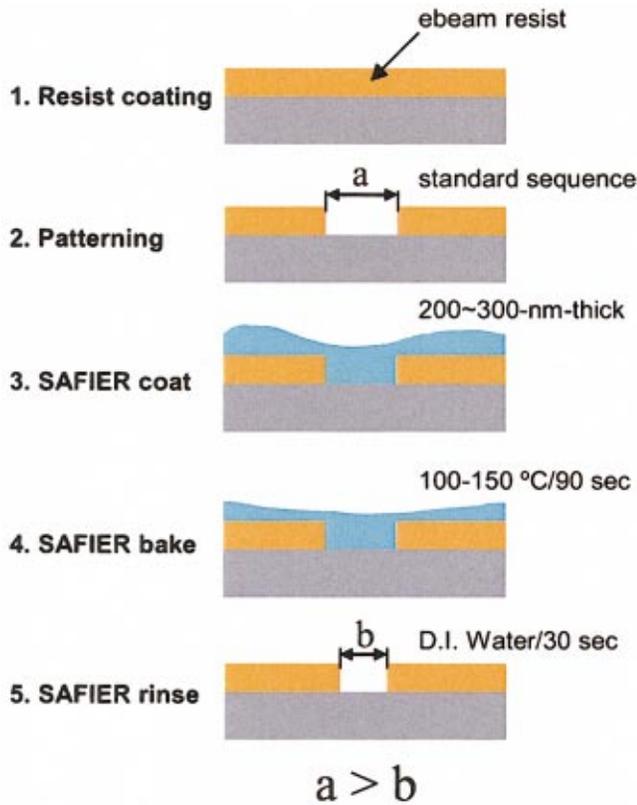


FIG. 1. SAFIER™ process flow.

III. RESULTS AND DISCUSSION

SAFIER™ process is a post-development treatment designed to shrink trench or contact hole patterns based on the thermal flow of photoresist with the use of special top-coating materials. Figure 1 shows the process flow. Up to process flow 2, standard resist patterning is done, followed by the top-coating of FSC-8000GM material in process flow 3 with a film thickness of 200–300 nm. Process flow 4 shows the baking process with temperatures at 100–160 °C for 60–90 s, and rinsing with deionized water. Figure 2

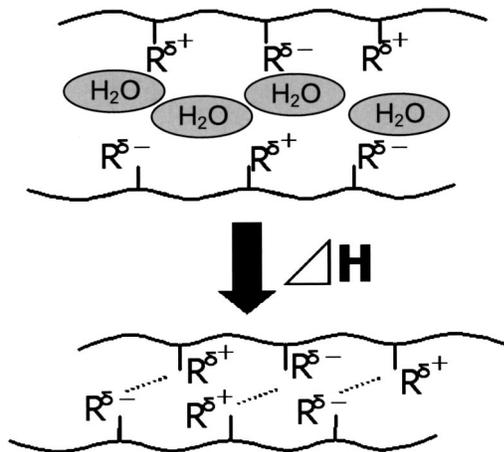


FIG. 2. SAFIER™ shrink mechanism.

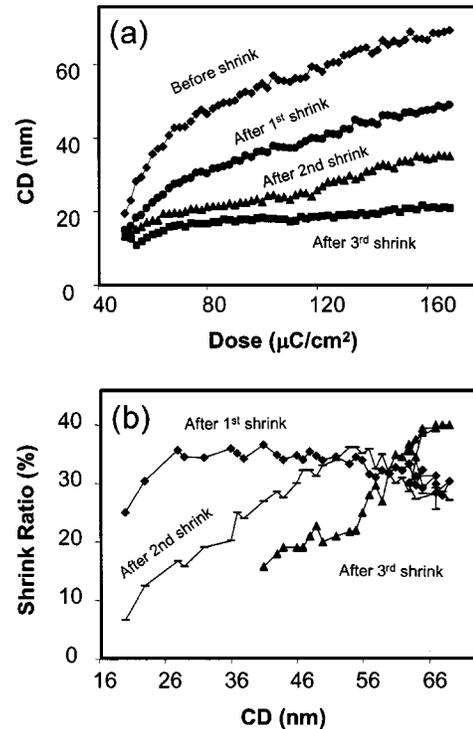


FIG. 3. Top pole trench in a 0.30- μm -thick UV113 resist with SAFIER™ processing at 120 °C for 90 s. (a) CDs vs dose, and (b) CDs vs shrink ratio.

shows the shrink mechanism.⁷ There are positively and negatively charged functional groups in the top-coating material of FSC-8000GM. The positively and negatively charged functional groups can interact with each other indirectly through the easily polarized medium—H₂O in this case. The following bake process evaporates the H₂O out of the top-coating material that allows the partially positively and negatively charged functional groups to have direct interactions. Such direct interactions make the top coating materials hold the resist profile during the resist thermal expands. This process allows us to keep the resist sidewall vertical in a predefined pattern while shrinking the resist gap.

One of the advantages of the SAFIER™ process is the flexibility to do multiple shrinkages. Multiple shrinks can be repeated on the same resist feature until the targeted dimension, e.g., trench width, is achieved without inducing much resist deterioration. The repetition evaluation experiments were performed with two different processing paths. The first path is to coat the post-developed wafer with the top-coating material, and then repeat the “bake-chill” processing cycle for multiple shrinks. After running this cycle multiple times, the wafer was finally rinsed with deionized water. The second path is to use “coat-bake-chill-rinse” as one single-process cycle, and then repeat this cycle multiple times. The experimental results show that there are no significant effects in improving resolution from the first path, but we did see a significant decrease in trench CD from the second path. Figure 3(a) shows the CD data of top pole trenches as a function of exposure dose before and after multiple shrinks. The CDs clearly decreased as the shrink cycles increased. The CD

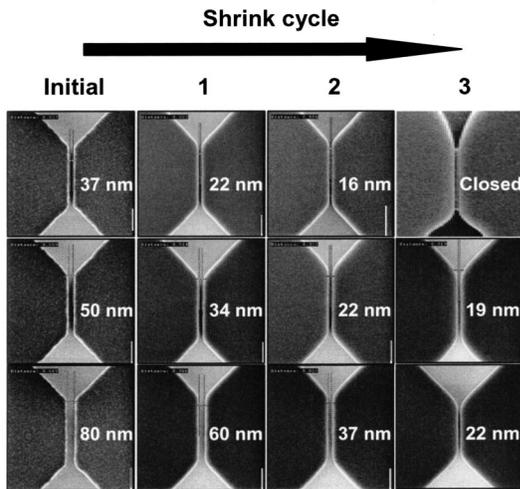


FIG. 4. SEM images of top pole trench in a 0.30- μm -thick UV113 resist before and after SAFIER™ processing (bake at 120 °C for 90 s) with multiple shrink cycle times.

curve became flat after 3 shrinkage cycles, indicating that all trench CDs were shrunk down to a ~ 20 nm region in a 0.30 μm resist. Based on the amount of CD shrinkage, we were able to establish the shrink ratio ($\Delta\text{CD}/\text{CD}$) as a function of CD, as shown in Fig. 3 (b). These data indicated that the shrink ratio is trench size dependent. As a result of the shrink process, Fig. 4 shows a series of SEM images of top pole trenches after CD shrink with multiple-shrink cycle times. All trench CDs regardless of initial size were shrunk down to a ~ 20 nm region, depending on how many shrink cycles were performed. High-resolution SEM images (not shown here) also show that the bottom of the trenches were cleared of resist residue since we used the CD shrinkage approach that allows us to initially use a higher dose to clear the trenches first and then decrease CD. Small amounts of resist residue are commonly seen in a high-AR narrow trench, which typically is difficult to completely remove for several reasons.⁴

To understand CD variation and LER using the SAFIER™ process, we did systematic measurements. The results are shown in Fig. 5. Both SEM images and CD mea-

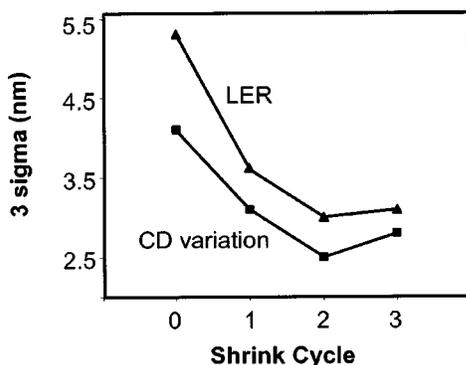


FIG. 5. 3-sigma of trench LER and CD variation vs shrink cycle times in a 0.30- μm -thick UV113 resist with SAFIER™ processing at 120 °C for 90 s.

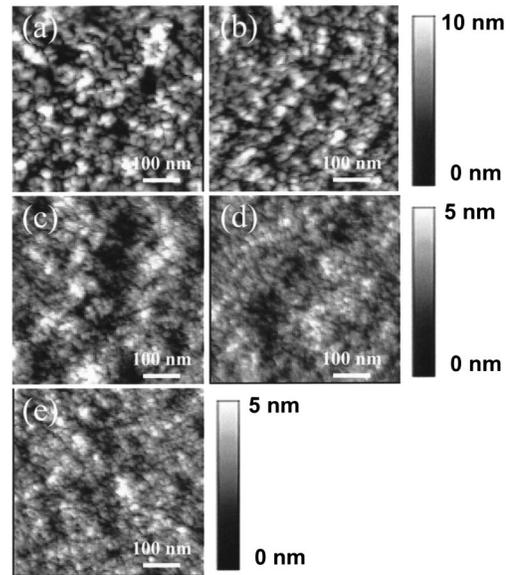


FIG. 6. AFM images of 0.30- μm -thick resist surfaces: (a) standard process without SAFIER™, (b) standard process with thermal flow treatment at 120 °C for 90 s, (c) standard process with one SAFIER™ shrink cycle, (d) standard process with two SAFIER™ shrink cycles, and (e) standard process with three SAFIER™ shrink cycles.

surements show that the SAFIER™ process can actually smooth the LER of the trench. This is extremely useful because LER degrades the lithographic resolution and linewidth accuracy for small CDs. We see that the CD variation and LER 3-sigma numbers significantly decrease after the first two shrink cycles, but stays flat or goes back up a little after the second shrink. This is because all the features were already shrunk down to the very narrow region at the length scale of sub-20 nm, in which measurement noise started to come from the CD measurements. We also took AFM images to see how the surface morphology changes with different processing treatments. Figure 6 shows the AFM images, and the results indicate that the SAFIER™ process smooths the surface of the resist. Figure 6(a) was the surface of a 0.30- μm -thick UV113 resist after standard processing without SAFIER™ processing. It shows surface roughness of 1.75 nm in root-mean-square (rms). Figure 6(b) is the surface of a 0.30- μm -thick UV113 resist after standard processing and then a thermal flow bake, but without applying SAFIER™ coating material. We noted that Fig. 6(b) shows a very similar structure and surface roughness of 1.81 nm as was seen in Fig. 6(a). However, we observed a totally different feature on the resist surface after SAFIER™ processing, as shown in Figs. 6(c)–6(e). Figures 6(c)–6(e) show three images of resist surfaces after SAFIER™ processing with shrink repetition cycles of 1 to 3 times, and their surface roughness of 0.785, 0.481, and 0.483 nm, respectively. All three of these images showed much smoother surfaces compared with those of Figs. 6(a) and 6(b). This observation suggests that the top-coating material does smooth the size of polymer resist aggregates

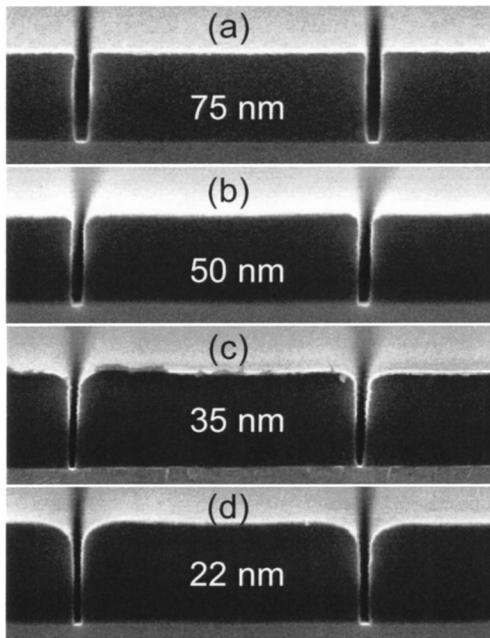


FIG. 7. Cross-sectional SEM images of trench in a 0.60- μm -thick UV113 resist before and after SAFIER™ processing (bake at 120 °C for 90 s) with multiple shrink cycle times.

during the bake-and-develop processing. We also noticed that there was not much change in surface roughness after the second shrink.

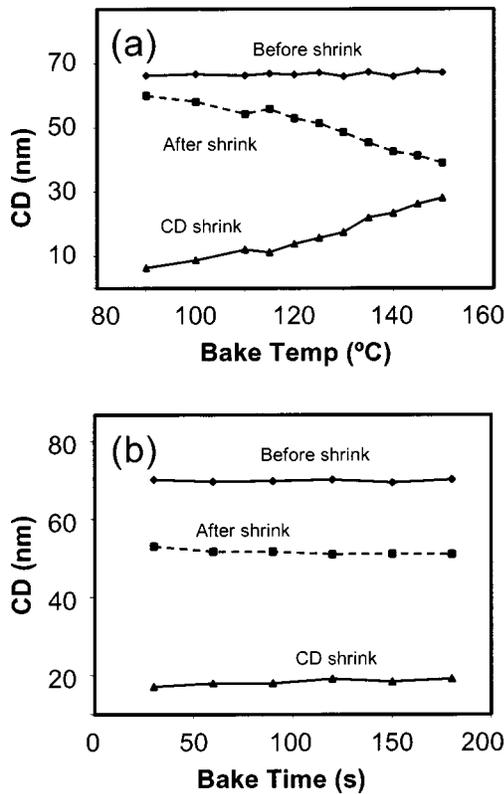


FIG. 8. Top pole trench in a 0.30- μm -thick UV113 resist with SAFIER™. (a) CDs vs bake temperature (°C) and (b) CDs vs bake time (s).

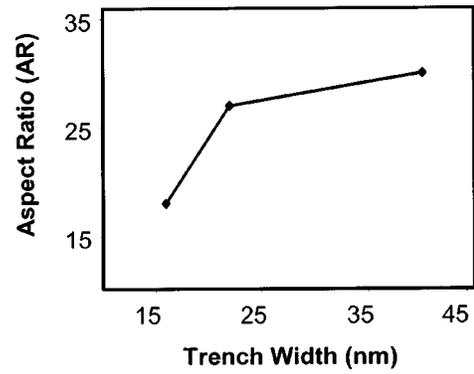


FIG. 9. Top pole trench CDs vs AR in UV113 resist with SAFIER™ process.

Another interesting aspect about the SAFIER™ process is how the resist profile of the narrow trench changes after

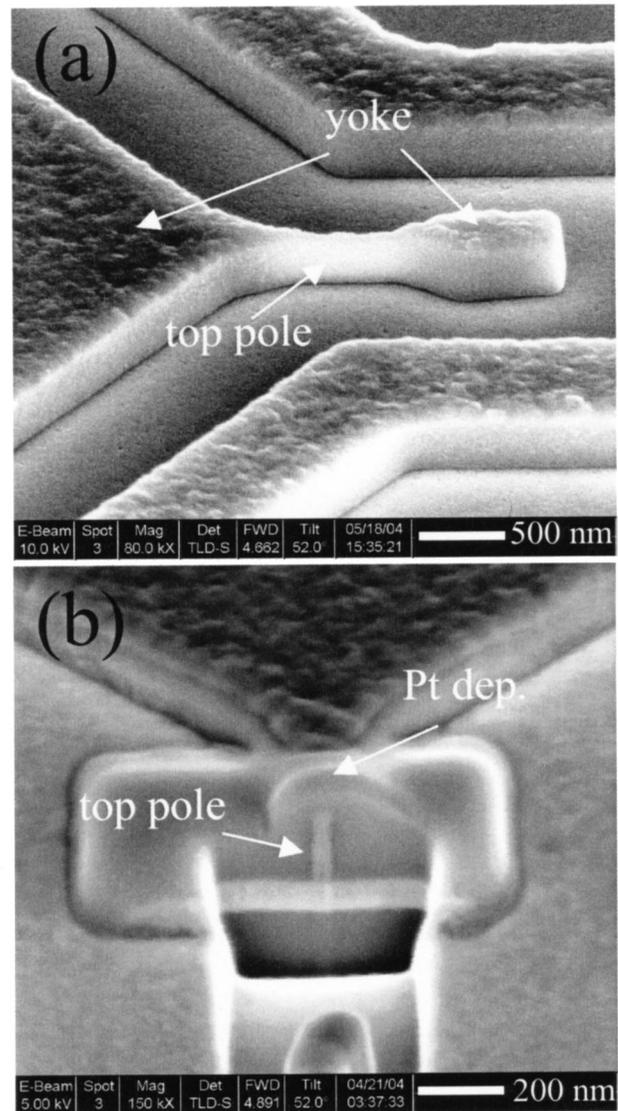


FIG. 10. (a) SEM image and (b) FIB cross-sectional SEM image of top pole structures plated with 2.4 T CoFe. Pole CD is 50 nm with an AR of ~10:1.

shrink. Figure 7 shows cross-sectional SEM images of 0.60- μm -thick resist trenches after SAFIER™ processing with multiple shrinks of 1 to 3 times. Figure 7(a) is the resist profile of the initial trench before shrink, and Figs. 7(b)–7(d) are the trenches after being shrunk 1 to 3 times, respectively. All images show that the sidewalls remain vertical even after the third shrink cycle. However, the top of the resist becomes more rounded with the increased number of shrink cycles.

We did CD shrink-sensitivity experiments regarding process conditions, such as bake temperatures and bake times. We found that adjusting the bake temperature was one of the most critical parameters that affected how much the trench shrunk. Figure 8(a) shows how the bake temperature affected CD shrinkage. As bake temperature increases, the CDs decrease accordingly at a rate of 0.4 nm/°C. Figure 8(b) shows how the bake time affected CDs. The results show that CD shrinkage is not sensitive to different bake times (only 0.7 nm/min) at a bake temperature of 125 °C. Figure 9 shows pole trench CDs as a function of resist thickness by means of electron-beam SAFIER™ process. We were able to print sub-20 nm top pole structures in a 0.30- μm -thick resist (AR = ~15:1), and electroplated top pole structures of 50 nm in a 0.50- μm -thick resist (AR = 10:1, shown in Fig. 10).

IV. CONCLUSION

We have coupled the SAFIER™ process to the top pole process for the purpose of fabricating thin-film heads. The

experimental results show that the SAFIER™ process not only shrinks the size of the trench, but also improves the LER of the trench, especially for narrow trenches. Therefore, the across-wafer CD variation of the trenches decrease after shrink. With our electron-beam SAFIER™ process, we demonstrated the capability of printing top pole structures with pole widths of sub-20 nm in a 0.30- μm -thick resist (AR > 15:1), and electroplated top pole structures of 50 nm in a 0.50- μm -thick resist (AR = 10:1). Ongoing work consists of the evaluation of wafer-to-wafer CD variation and overlay alignment accuracy of critical features with electron-beam SAFIER™ process.

ACKNOWLEDGMENTS

The authors would like to thank Nicholas Katchur and Katsumi Omori of TOK OHKA America for their sample supply and very helpful discussions.

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